IN THE CLAIMS

Presented below are the claims as they presently stand.

1. An MOS device comprising:

a gate dielectric formed on first conductivity region of a substrate;

a gate electrode formed on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type formed in said substrate and on opposite sides of said gate electrode and creating inflection points beneath said gate electrode and said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions extend beneath the gate electrode and define a channel region beneath said gate electrode in said first conductivity type region, and wherein said channel region directly beneath said gate electrode is larger than said channel region between said inflection points.

2. The MOS device of claim 1 wherein said silicon or silicon alloy source/drain regions extend above said gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric.

3. The MOS device of claim 1 wherein said gate dielectric layer is thicker beneath outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode.

4. The MOS device of claim 2 wherein said gate dielectric layer is thicker beneath said sidewall spacer and said outside edge of said gate electrode then the gate dielectric layer beneath the center of said gate electrode.

5. The MOS device of claim 1 further comprising a pair of silicon or silicon alloy regions having a first conductivity type region formed between said pair of silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region.

6. The MOS device of claim 5 wherein the concentration of said silicon or silicon alloy regions having a first conductivity type is greater than the concentration of said first conductivity type region.

7. The MOS device of claim 1 wherein said silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said gate electrode at said inflection points which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-200Å beneath said gate dielectric.

8. The MOS device of claim 1 wherein said first conductivity type is n-type conductivity and wherein said second conductivity type is p-type conductivity.

9. The MOS device of claim 1 wherein said first conductivity type is p-type conductivity and wherein said second conductivity type is n-type conductivity.

10. The MOS device of claim 1 wherein the concentration of said silicon or silicon alloy source/drain regions of a second conductivity type have a concentration between $1x10^{18}/cm^3 - 3x10^{21}/cm^3$.

11. The MOS device of claim 10 wherein the concentration of said silicon or silicon alloy source/drain regions of a second conductivity type is approximately $1x10^{21}/cm^3$.

12. The MOS device of claim 1 further comprising silicide formed on said silicon or silicon alloy source/drain regions.

13. An MOS device comprising:

a gate dielectric formed on a first conductivity type region of a substrate;

a gate electrode formed on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of silicon-germanium alloy source/drain regions having a second conductivity type formed in said substrate and along opposite sides of said gate electrode wherein said silicon-germanium alloy silicon-germanium alloy source/drain region in said substrate are inwardly concaved and create an inflection point in said substrate, said silicon germanium alloy extends above the height of said gate dielectric layer wherein the top surface of said deposited silicon or silicon alloy is spaced further from said gate electrode than said silicon or silicon alloy adjacent to said gate dielectric.

14. The MOS device of claim 13 wherein said gate dielectric layer is thicker beneath said outside edges of said gate electrode then the gate dielectric beneath the center of the gate electrode.